

# DATA SHEET

**PDI1284P11**

**3.3V Parallel interface transceiver/buffer**

Product specification  
Supersedes data of 1997 Sep 15

1999 Sep 17

## 3.3V Parallel interface transceiver/buffer

## PDI1284P11

### FEATURES

- Asynchronous operation
- 8-Bit transceivers
- 6 additional buffer/driver lines peripheral to cable
- 5 additional control lines from cable
- 5V tolerant
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model
- Latch up protection exceeds 500 mA per JEDEC Std 19
- Input Hysteresis
- Low Noise Operation
- IEEE 1284 Compliant Level 1 & 2
- Overvoltage Protection on B/Y side for OFF-state
- A side 3-State option
- B side active or resistive pull up option
- Cable side  $V_{CC}$  for 5V or 3V operation

### DESCRIPTION

The PDI1284P11 parallel interface chip is designed to provide an asynchronous, 8-bit, bi-directional, parallel interface for personal computers. The part includes all 19 signal lines defined by the IEEE1284 interface specification for Byte, Nibble, EPP, and ECP modes. The part is designed for hosts or peripherals operating at 3.3V to interface 3.3V or 5.0V devices.

The 8 transceiver pairs (A/B 1-8) allow data transmission from the A bus to the B bus, or from the B bus to the A bus, depending on the state of the direction pin DIR.

The B bus and the Y9-Y13 lines have either totem pole or resistor pull up outputs, depending on the state of the high drive enable pin HD. The A bus has only totem pole style outputs. All inputs are TTL compatible with at least 400mV of input hysteresis at  $V_{CC} = 3.3V$ .

### QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS $T_{amb} = 25^{\circ}C$ ; $GND = 0V$	TYPICAL	UNIT
$R_D$	B/Y Side output resistance	$V_{CC} = 3.3V$ ; $V_O = 1.65V \pm 0.2V$ (See Figure 2)	45	$\Omega$
$R_{PU}$	B/Y side pull up resistance	$V_{CC} = 3.3V$ ; Outputs, resistive pull up	1.4K	$\Omega$
SR	B/Y Side slew rate	$R_L = 62\Omega$ ; $C_L = 50pF$ (See Waveform 4)	0.2	V/ns
$I_{CC}$	Total static current	$V_I = V_{CC}/GND$ ; $I_O = 0$	5	$\mu A$
$V_{HYS}$	Input hysteresis	$V_{CC} = 3.3V$	0.47	V
$t_{PLH}/t_{PHL}$ A –B/Y	Propagation delay to the B/Y side outputs	$V_{CC} = 3.3V$	12.5/13.9	ns

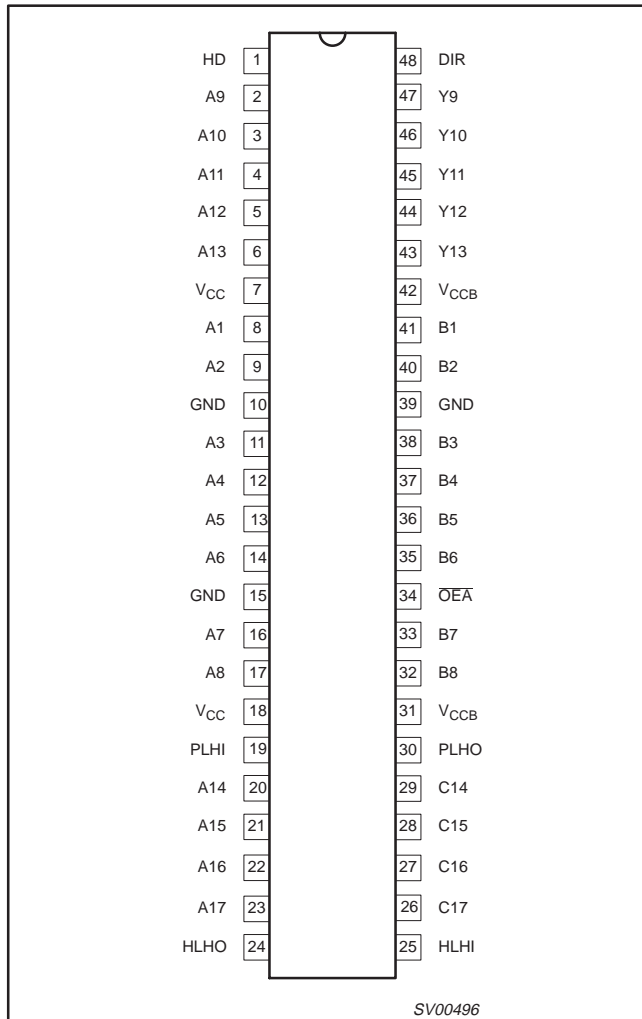
### ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
48-pin plastic SSOP Type II	0°C to +70°C	PDI1284P11 DL	SOT370-1
48-pin plastic TSSOP Type II	0°C to +70°C	PDI1284P11 DGG	SOT362-1

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#### PIN CONFIGURATION



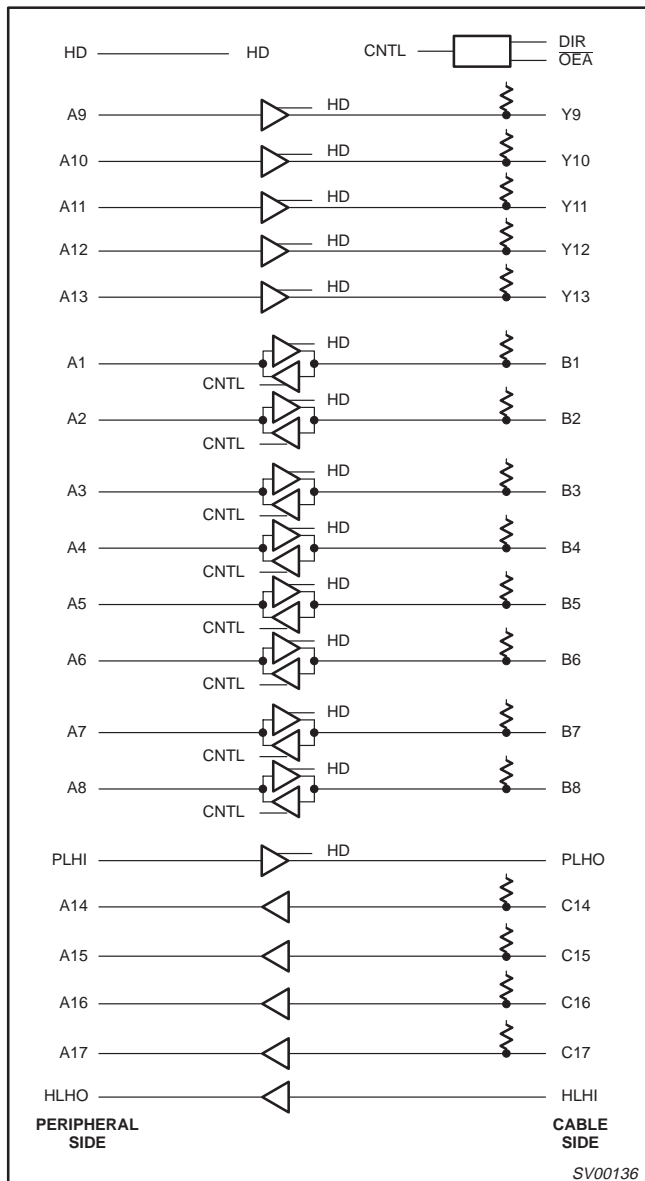
#### PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
8, 9, 11, 12, 13, 14, 16, 17	A1 - A8	Data inputs/outputs
41, 40, 38, 37, 36, 35, 33, 32	B1 - B8	IEEE 1284 Std. outputs/inputs
2, 3, 4, 5, 6	A9 - A13	Data inputs
47, 46, 45, 44, 43	Y9 - Y3	IEEE 1284 Std. outputs
29, 28, 27, 26	C14 - C17	Control inputs (cable)
20, 21, 22, 23	A19 - A17	Control outputs (peripheral)
1	HD	B/Y-side high drive enable/disable
48	DIR	Direction selection A to B / B to A
19	PLHI	Peripheral logic high input (peripheral)
30	PLHO	Peripheral logic high output (cable)
25	HLHI	Host logic high input (cable)
24	HLHO	Host logic high output (cable)
10, 15, 39	GND	Ground (0V)
7, 18	V <sub>CC</sub>	Positive supply voltage
31, 42	V <sub>CCB</sub>	Cable side power supply voltage 3V/5V
34	OE $\bar{A}$	A side output enable

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#### LOGIC SYMBOL



#### FUNCTION TABLE

DIR	$\overline{OE\bar{A}}$	HD	INPUTS	OUTPUTS	OUTPUT TYPES
X	X	X	C14-17	A14-17	$t_P$
X	X	X	HLHI	HLHO	$t_P$
X	X	L	A9-13	Y9-13	$r_P$
X	X	H	A9-13	Y9-13	$t_P$
X	X	L	PLHI	PLHO	O.C.
X	X	H	PLHI	PLHO	$t_P$
H	X	L	A1-8	B1-8	$r_P$
H	X	H	A1-8	B1-8	$t_P$
L	L	X	B1-8	A1-8	$t_P$
L	H	X		A1-8	Z*
L	H	X	B1-8		$r_P^*$

A = Side driving internal IC  
 B = Side driving external cable (bidirectional)  
 C = Side receiving control signals from internal cable  
 Y = Side driving external cable (unidirectional)  
 X = Don't care – control signals in  
 Z = High Z or 3-State  
 O.C.= Open collector  
 $t_P$  = Totem pole output  
 $r_P$  = Resistive pull up: 1.4k $\Omega$  (nominal) on B/Y/C cable side and  $V_{CC}$ . However, while a B/Y side output is Low as driven by a Low signal on the A side, that particular B/Y side resistor is switched out to stop current drain from  $V_{CC}$  through it.  
 \* When DIR = L and  $\overline{OE\bar{A}}$  = H, the output signal is isolated from the input signal. B1 – 8 signals maintain an  $r_P$  = 1.4k $\Omega$  on the input for this mode.

#### PINS WITH PULL UP RESISTORS TO LOAD CABLE

PINS	SYMBOL	FUNCTION
47, 46, 45, 44, 43	Y9 – Y13	Output cable drivers
41, 40, 38, 37, 36, 35, 33, 32	B1 – B8	Output cable drivers
29, 28, 27, 26	C14 – C17	External cables control signal input

## 3.3V Parallel interface transceiver/buffer

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**ABSOLUTE MAXIMUM RATINGS<sup>1, 2</sup>**

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
	ESD Immunity, per Mil Std 883C method 3015		±1	kV
V <sub>CC</sub>	DC supply voltage		-0.5 to +4.6	V
V <sub>CCB</sub>	DC cable supply voltage		-0.5 to +6.5	V
I <sub>IK</sub>	DC input diode current	V <sub>I</sub> < 0	±20	mA
I <sub>OK</sub>	DC output diode current	V <sub>O</sub> < 0	±50	mA
V <sub>IN</sub>	DC input voltage <sup>3</sup>		-0.5 to +5.5	V
V <sub>OUT B/Y</sub>	DC output voltage on B/Y side <sup>3</sup>		-0.5 to +5.5	V
V <sub>OUT B/Y</sub>	Transient output voltage on B/Y side <sup>4</sup>	40ns transient	-2 to +7	V
V <sub>OUT A</sub>	DC output voltage on A side		-0.5 to V <sub>CC</sub> + 0.5	V
I <sub>O</sub>	DC output current	Outputs in High or Low state	±50	mA
T <sub>stg</sub>	Storage temperature range		-60 to +150	°C
I <sub>CC</sub> /I <sub>GND</sub>	Continuous current through V <sub>CC</sub> or GND		±200	mA

**NOTES:**

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
- V<sub>OUT B/Y</sub> (tr) guarantees only that this part will not be damaged by reflections in application so long as the voltage levels remain in the specified range.

**RECOMMENDED OPERATING CONDITIONS**

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V <sub>CC</sub>	DC supply voltage	3.0	3.6	V
V <sub>CCB</sub>	DC cable supply voltage	3.0	5.5	V
V <sub>IH</sub>	High level Input voltage	2.0		V
V <sub>IL</sub>	Low level input voltage		0.8	V
V <sub>OUT B/Y</sub>	B/Y output voltage	-0.5	5.5	V
V <sub>OUT A</sub>	A side output voltage	0	V <sub>CC</sub>	V
I <sub>OH</sub>	B/Y side output current High		-14	mA
I <sub>OL</sub>	B/Y side output current Low		14	mA
T <sub>amb</sub>	Operating free-air temperature range	0	+70	°C

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## DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			$T_{amb} = 0^{\circ}\text{C to } 70^{\circ}\text{C}$			
			MIN	TYP	MAX	
$V_{HYS, A, B}$	Input hysteresis	A, B, control inputs, $V_{CC} = 3.3\text{V}$ , $V_{IL} = 0.8$ , $V_{IH} = 2.0$	0.4			V
$V_{IH, A, B, PLHI}$	High-level input voltage	$V_{CC} = 3.0$ to $3.6\text{V}$	2.0			V
$V_{IL, A, B, PLHI}$	Low-level input voltage	$V_{CC} = 3.0$ to $3.6\text{V}$			0.8	V
$V_{HYS, C}$	Input hysteresis	C Inputs, $V_{CC} = 3.3\text{V}$	0.8			V
$V_{IH, C}$	High-level input voltage	C Inputs, $V_{CC} = 3.0$ to $3.6\text{V}$	2.3			V
$V_{IL, C}$	Low-level input voltage	$V_{CC} = 3.0$ to $3.6\text{V}$			0.8	V
$V_{IH, HLH}$	High-level input voltage	$V_{CC} = 3.6\text{V}$	2.6			V
$V_{IL, HLH}$	Low-level input voltage	$V_{CC} = 3.0$			1.55	V
$R_{DP}$	Output impedance	$V_{CC} = 3.3\text{V}$ , $V_O = 1.65 \pm 0.1\text{V}$ See Fig. 2	35	45	55	$\Omega$
$R_{DN}$	Output impedance	$V_{CC} = 3.3\text{V}$ , $V_O = 1.65 \pm 0.1\text{V}$ See Fig. 2	35	45	55	$\Omega$
$R_{PU}$	Pull up resistance	$V_{CC} = 3.3\text{V}$ , outputs in high Z	1.15	1.4	1.65	k $\Omega$
$V_{OH, B/Y}$	High-level output voltage	$V_{CC} = 3.0\text{V}$ , $I_{OH} = -14\text{mA}$	2.23			V
$V_{OL, B/Y}$	Low-level output voltage	$V_{CC} = 3.0\text{V}$ , $I_{OL} = 14\text{mA}$			0.77	V
$V_{OH, A}$ and HLH	High-level output voltage	$I_{OH} = -500\mu\text{A}$ , $V_{CC} = 3.0\text{V}$	2.8			V
		$I_{OH} = -4\text{mA}$ , $V_{CC} = 3.0\text{V}$	2.4			
$V_{OL, A}$ and HLH	Low-level output voltage	$I_{OL} = 50\mu\text{A}$ , $V_{CC} = 3.0\text{V}$			0.2	V
		$I_{OL} = 4\text{mA}$ , $V_{CC} = 3.0\text{V}$			0.4	
$V_O$ PLH	High-level output voltage	$I_{OH} = 500\mu\text{A}$ , $V_{CC} = 3.15\text{V}$	3.1			V
	Low-level output voltage	$I_{OL} = 500\mu\text{A}$ , $V_{CC} = 3.0\text{V}$			0.8	
$I_{CC}$	Quiescent supply current for $V_{CC}$ and $V_{CCB}$ under all conditions except when B or C inputs are LOW	$V_{CC} = 3.6\text{V}$ , $V_{CCB} = 3.6\text{V to } 5.5\text{V}$ $V_{in} = 0$ or $V_{CC}$ ; $V_{Bin} = V_{CCB}$ $V_{cin} = V_{CCB}$ or Floating		0.1	100	$\mu\text{A}$
$I_{CCBL}^2$	Quiescent supply current for $V_{CCB}$ when B or C inputs are LOW	$V_{CC} = V_{CCB} = V_{dir} = 3.6\text{V}$ $V_{in} = 0$ or $V_{CC}$ ; $V_{cin} = 0\text{V}$		10	15	mA
		$V_{CC} = V_{dir} = 3.6\text{V}$ ; $V_{CCB} = 5.5\text{V}$ $V_{in} = 0$ or $V_{CC}$ ; $V_{cin} = 0\text{V}$		16	20	
		$V_{CC} = V_{CCB} = 3.6\text{V}$ ; $V_{dir} = 0\text{V}$ $V_{in} = 0$ or $V_{CC}$ ; $V_{Bin} = V_{cin} = 0\text{V}$		30	40	
		$V_{CC} = 3.6\text{V}$ , $V_{CCB} = 5.5\text{V}$ ; $V_{dir} = 0\text{V}$ $V_{in} = 0$ or $V_{CC}$ ; $V_{Bin} = V_{cin} = 0\text{V}$		47	60	
$I_{off}$ C/B/Y side	Power off leakage current	$V_O = 5.5\text{V}$ , $V_{CC} = V_{CCB} = 0$			+100	$\mu\text{A}$
		$V_O = 5.5\text{V}$ , $V_{CC} = 0$ , $V_{CCB} = 4.5\text{V}$			$\pm 100$	
$I_{in}^1$	Input leakage current	Input leakage current <sup>1</sup> $V_{in} = 0$ to $V_{CC}$			$\pm 1$	$\mu\text{A}$
$I_{OZ}^1$	3-State output current	$V_{OUT} = V_{CC}$ or GND			$\pm 20$	$\mu\text{A}$

## NOTES:

- The pull up resistor on the B side outputs makes it impossible to test  $I_{OZ}$  on the B side. This applies to the input current on the C side inputs as well.
- Includes extra ICCB current from pull-up resistors, i.e.  $ICCB = (\#B + \#C \text{ LOW inputs}) * (V_{CCB}/R_{PU})$ .

## 3.3V Parallel interface transceiver/buffer

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**AC CHARACTERISTICS**GND = 0V,  $t_R = t_F = 3.0\text{ns}$ ,  $C_L = 50\text{pF}$ ,  $R_L = 500\Omega$ 

SYMBOL	PARAMETER	TEST CONDITIONS	WAVEFORMS	LIMITS			UNIT
				$T_{\text{amb}} = 0^\circ\text{C to } +70^\circ\text{C}$			
				MIN	TYP	MAX	
$t_{\text{PLH}}$	Propagation delay	Path A to B or Y	2, 5	0		20	ns
$t_{\text{PHL}}$				0		20	
$t_{\text{PLH}}$	Propagation delay	Path B to A	2, 5	0		12	ns
$t_{\text{PHL}}$				0		12	
$t_{\text{PLH}}$	Propagation delay	Path C to A	2, 5			15	ns
$t_{\text{PHL}}$						15	
$t_{\text{PLH}}$	Propagation delay	Path PLH	2, 5			20	ns
$t_{\text{PHL}}$						20	
$t_{\text{PLH}}$	Propagation delay	Path HLH	2, 5			15	ns
$t_{\text{PHL}}$						15	
$t_{\text{slew}}$	Slew rate	B or Y side outputs	4	0.05		0.4	V/ns
$t_{\text{PHZ}}$	Output enable/ disable time	HD to Y or B $R_L = 500\Omega$	3			20	ns
$t_{\text{PZH}}$						20	
$t_{\text{DIFF}}$	Propagation delay difference	HD prop $t_{\text{PZH}} - t_{\text{PHZ}}$				10	ns
$t_{\text{PHZ}}$	Output enable time	HD to PLHO $R_L = 500\Omega$	3			20	ns
$t_{\text{PZH}}$						20	
$t_{\text{PHZ}}$	Output enable/ disable time	Dir to B $R_L = 250\Omega$ on the B/Y side $t_p$ load	Fig 1.			50	ns
$t_{\text{PZH}}$						30	
$t_{\text{PLZ}}$						50	
$t_{\text{PZL}}$						30	
$t_{\text{PHZ}}$	Output enable/ disable time	Dir to A $R_L = 250\Omega$	1 Fig 1.			15	ns
$t_{\text{PZH}}$						50	
$t_{\text{PLZ}}$						15	
$t_{\text{PZL}}$						50	
$t_{\text{PHZ}}$	Output enable/ disable time	$\overline{\text{OE}}\text{A to A}$ $R_L = 250\Omega$	3 Fig 1.			6	ns
$t_{\text{PZH}}$						12	
$t_{\text{PLZ}}$						6	
$t_{\text{PZL}}$						12	

### 3.3V Parallel interface transceiver/buffer

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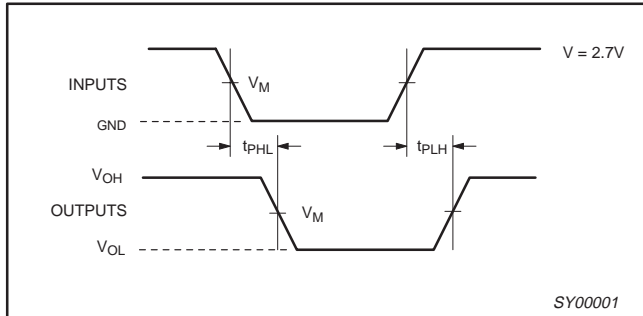
#### AC WAVEFORMS

$V_M = 1.5V$

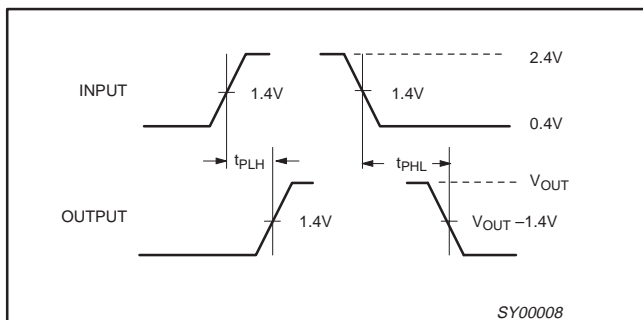
$V_X = V_{OL} \pm 0.3V$

$V_Y = V_{OH} - 0.3V$

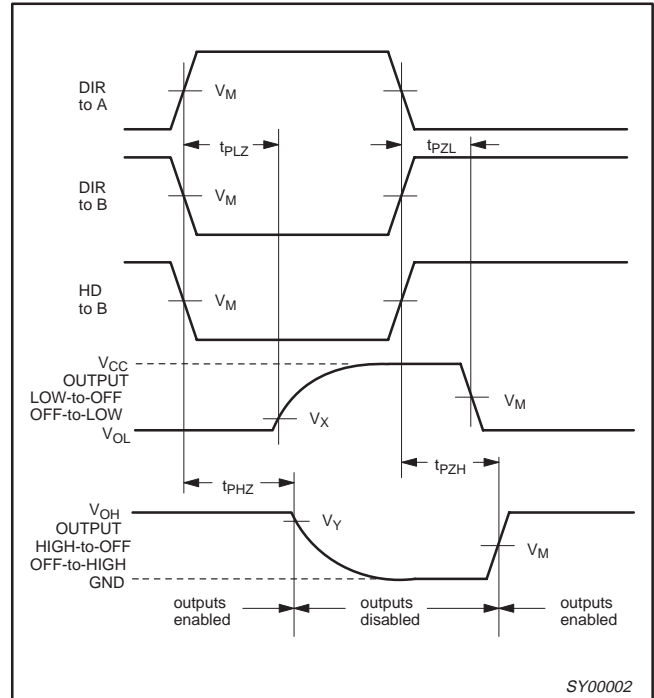
$V_{OL}$  and  $V_{OH}$  are the typical output voltage drops that occur with the output load. ( $V_{CC}$  never goes below 3.0V).



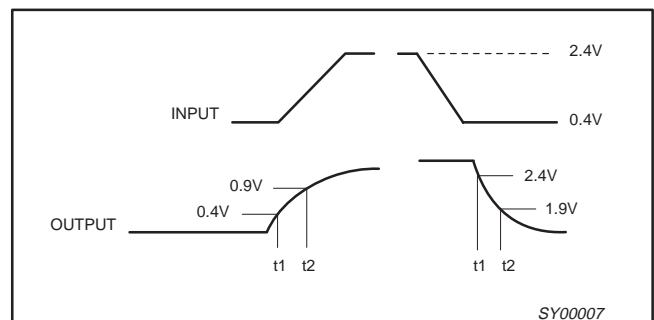
Waveform 1. Input Bn to output An propagation delays



Waveform 2. Voltage Waveforms Propagation Delay Times (A To B) Measured at Output Pin



Waveform 3. 3-State enable and disable times



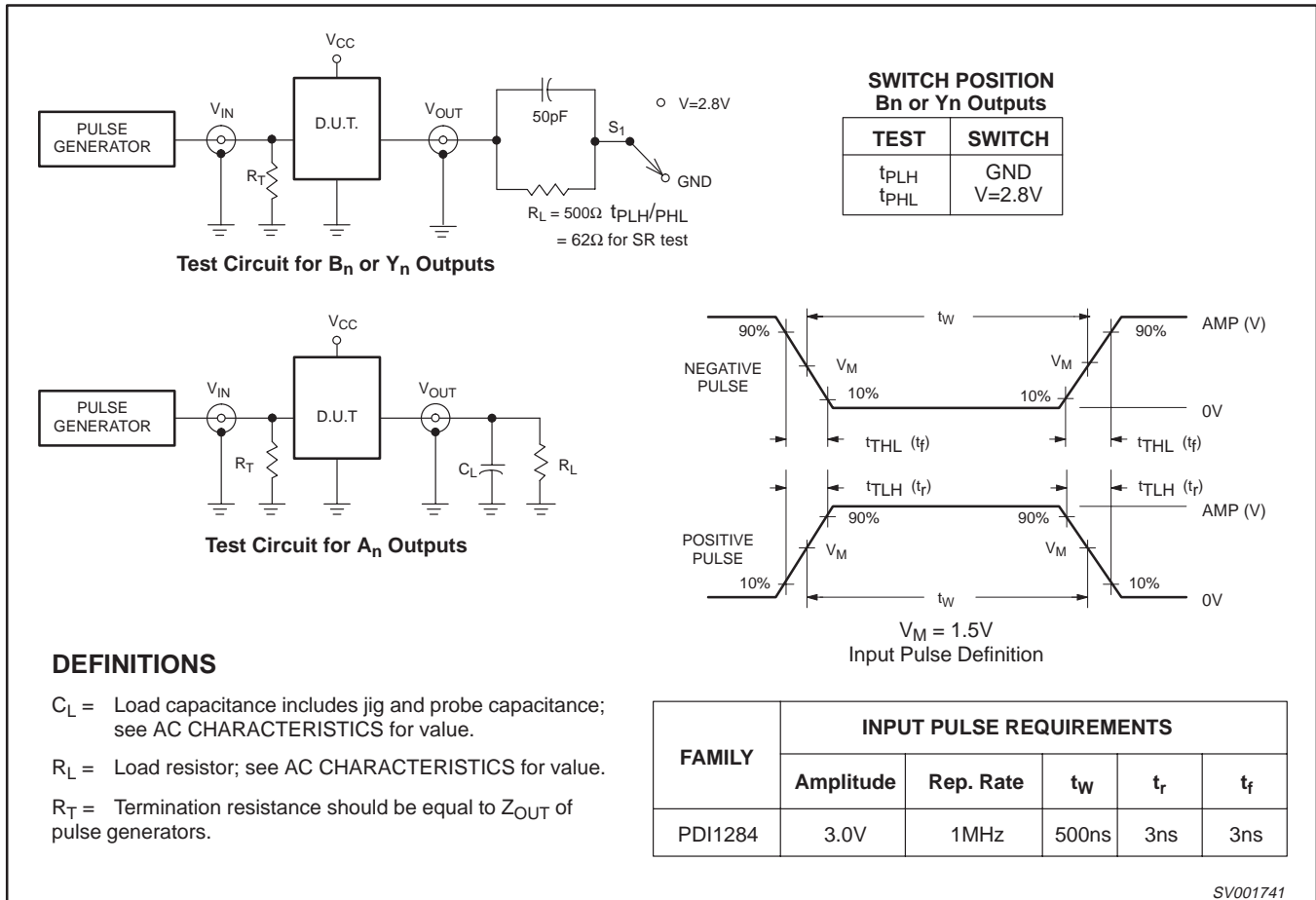
Waveform 4. Slew Rate Voltage Waveforms on B/Y side  
 (Input pulse rise and fall time are 3ns, 150ns < pulse width < 10 μs, for both a Low to High and a High to Low transition.)  
 Slew Rate measured between 0.4V and 0.9V - rising.  
 Slew Rate measured between 2.4V and 1.9V - falling.  
 Slew Rate measured at  $V_{OUT}$  as specified in Waveform 5.



# 3.3V Parallel interface transceiver/buffer

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## TEST CIRCUITS AND WAVEFORMS



SV001741

Waveform 5.

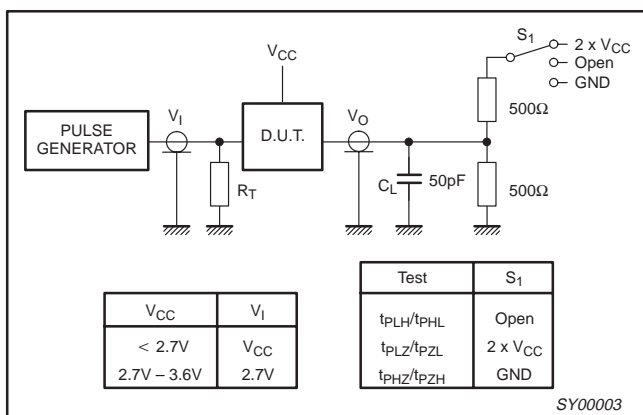


Figure 1. Load Circuitry for B<sub>n</sub> to A<sub>n</sub> Switching Times

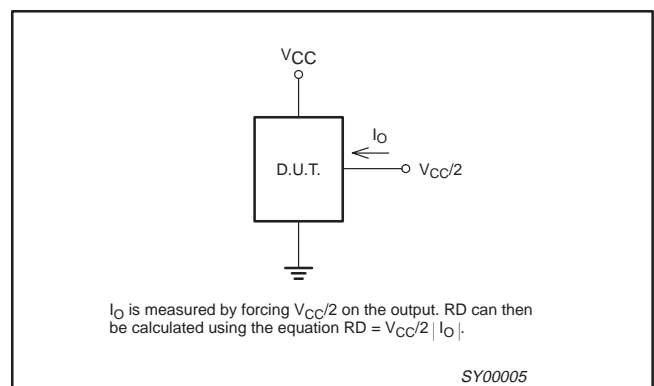


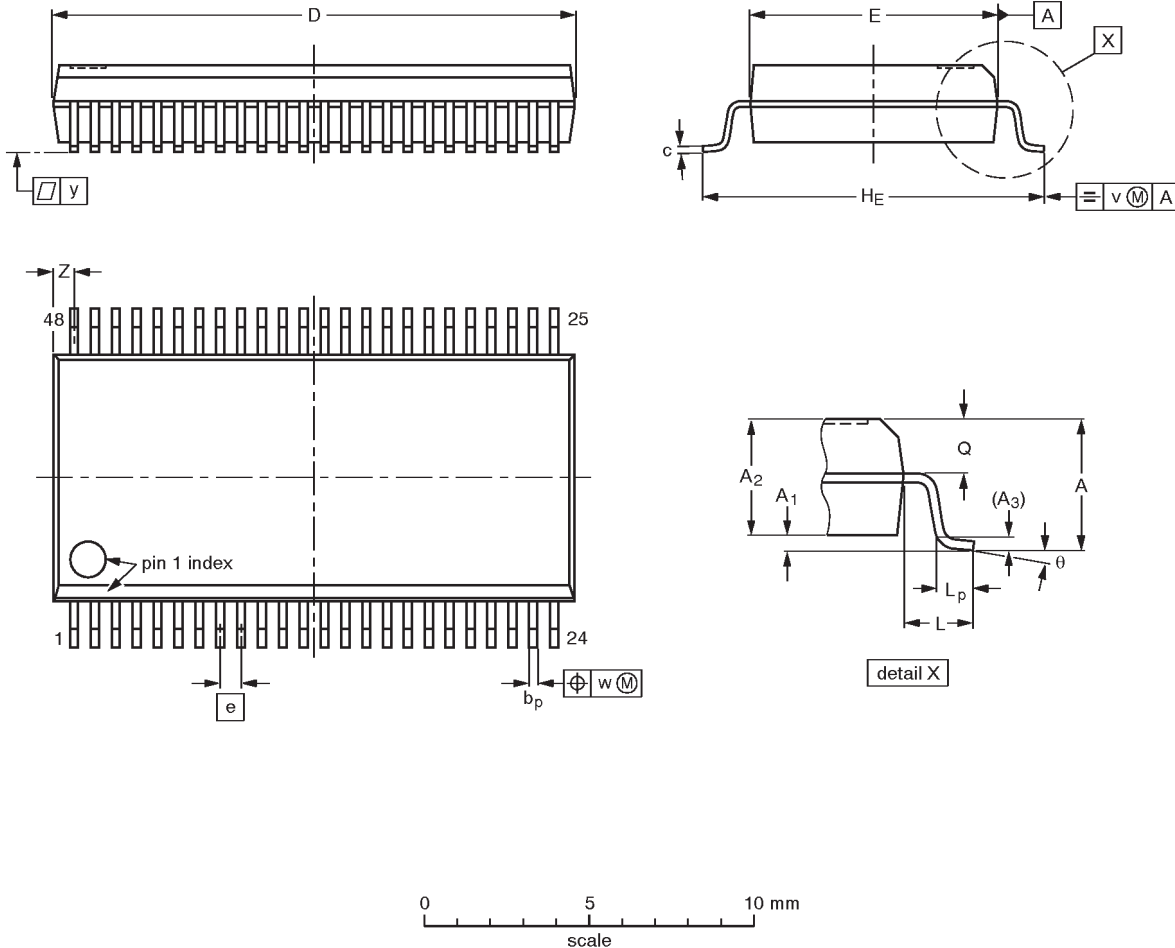
Figure 2. Output Impedance R<sub>D</sub>

# 3.3V Parallel interface transceiver/buffer

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**SSOP48:** plastic shrink small outline package; 48 leads; body width 7.5 mm

**SOT370-1**



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	2.8	0.4 0.2	2.35 2.20	0.25	0.3 0.2	0.22 0.13	16.00 15.75	7.6 7.4	0.635	10.4 10.1	1.4	1.0 0.6	1.2 1.0	0.25	0.18	0.1	0.85 0.40	8° 0°

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

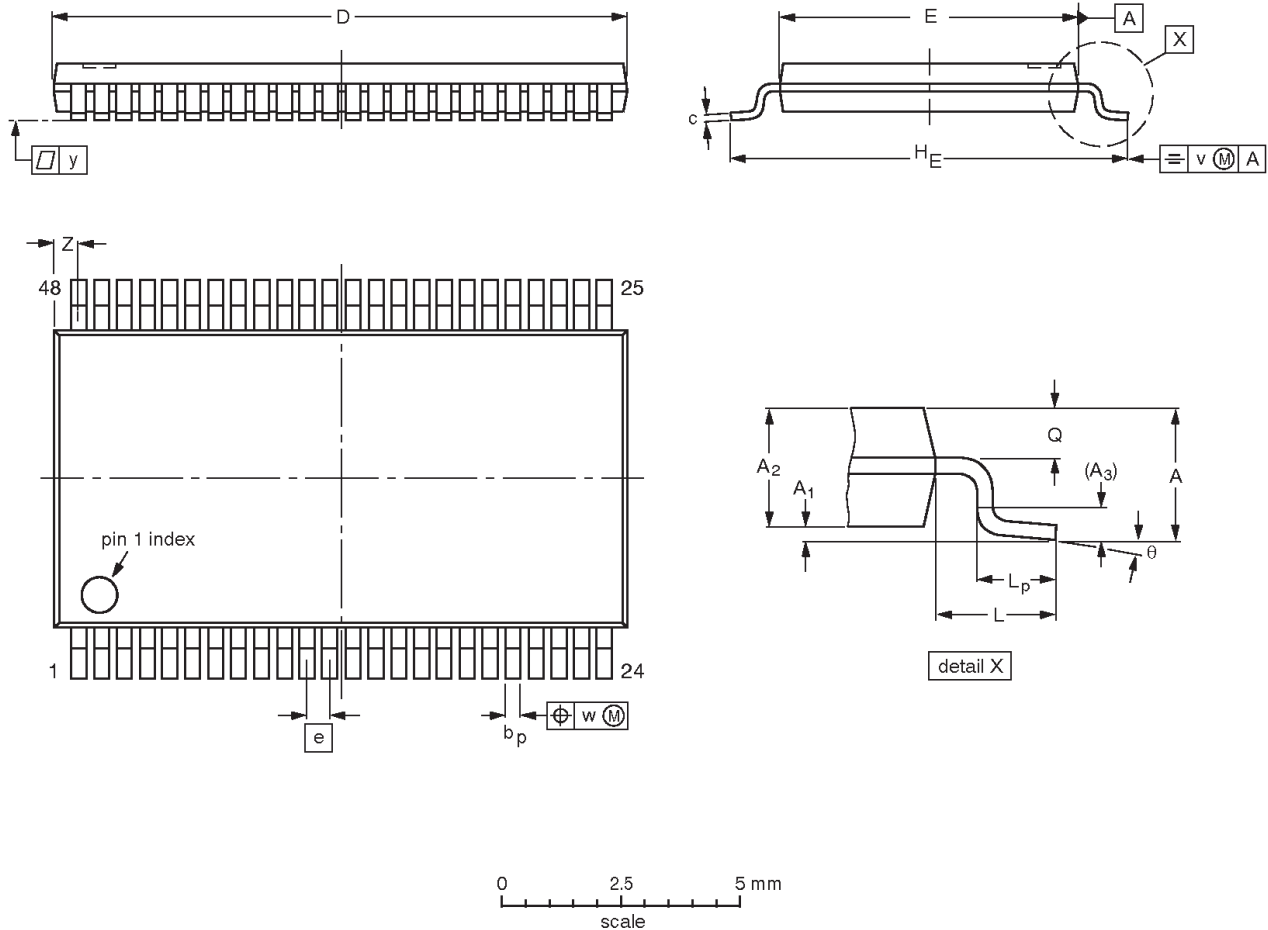
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT370-1		MO-118AA				93-11-02- 95-02-04

### 3.3V Parallel interface transceiver/buffer

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**TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1mm**

**SOT362-1**



**DIMENSIONS (mm are the original dimensions).**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	0.2 0.1	12.6 12.4	6.2 6.0	0.5	8.3 7.9	1	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.8 0.4	8° 0°

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT362-1		MO-153ED				93-02-03 95-02-10

## 3.3V Parallel interface transceiver/buffer

PDI1284P11

## Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

## Definitions

**Short-form specification** — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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Date of release: 09-99

Document order number:

9397 750 06421

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